Fully-Depleted SOI MOSFET Sensors in Accumulation Mode for Total Dose Measurement

Fabricio Alcalde Bessia, Denis Flandre, Nicolas André, Julieta Irazoqui, Martín Pérez, Mariano Gómez Berisso, and Jose Lipovetzky

***Abstract*—Fully Depleted Silicon-on-Insulator (FD-SOI) transistors fabricated with a custom process in *Université Catholique de Louvain* (UCL) were irradiated with X-rays using an Elekta Synergy radiotherapy linear accelerator. I-V curves of FD-SOI are sensitive to charges produced in the buried oxide (BOX) by ionizing radiation, so it is possible to use these devices as radiation dosimeters. In this work, we evaluated the use of thick BOX back-gate transistors for Total Ionizing Dose (TID) measurement using different bias conditions and we obtained a maximum sensitivity of 191 mV/Gy for devices operating in accumulation mode.**

***Index Terms*—Radiation Dosimeter, SOI**

I. Introduction

THe radiation-induced Threshold Voltage (V_T) shift of MOS transistors has been used for many years for the measurement of Total Ionizing Dose (TID). To obtain devices with sensitivities useful for space and radiotherapy applications, the gate oxide thicknesses must be greater than several hundreds of nanometers, which is usually obtained in ad-hoc processes [1], [2]. In the past years, several works proposed the use in dosimetry of transistors built using the Buried Oxide (BOX) available in Silicon On Insulator (SOI) processes, either using the V_{th} shift in the back-gate transistor [3], [4] or the shift in front gate transistors through body effect [5]. In this work, we evaluate the use of thick BOX back-gate transistors for TID measurement in a Fully Depeted (FD) SOI process, comparing accumulation-mode FD-SOI with inversion-mode FD-SOI devices.

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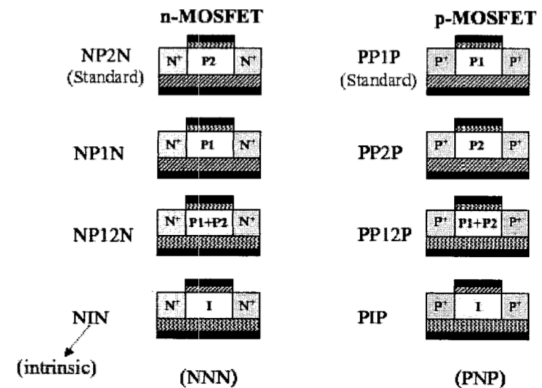

Fig. 1. FD-SOI MOS devices that were irradiated. The fabrication process allows different film dopings using 2 doping masks. Taken from [6].

II. Experimental Details

FD-SOI MOS transistors were irradiated using an Elekta Synergy Linear Accelerator (Linac) in a radiotherapy facility. The devices, depicted in Fig. 1, were fabricated in the *Université Catholique de Louvain* (UCL) clean-room using a fabrication process that was developed in-house [6]. These transistors have a gate oxide thickness of 31 nm, a 80 nm thick layer of silicon and a 400 nm thick buried oxide (BOX), built on SmartCut UNIBOND wafers. The gate is n^+-poly and the channel is doped with Boron in order to have accumulation operating mode p-MOSFETs and inversion operating mode n-MOSFETs. With the combination of two implant steps P1 and P2, it is possible to have different channel dopings, a very low B concentration (I), intermediate concentrations (P1 and P2) and a higher concentration (P12).

A test chip was fabricated containing all types of transistors with channel lengths of $20\,\mu\text{m}$ and widths of $20\,\mu\text{m}$. The die was encapsulated in a DIL24 ceramic package with open lid, each transistor was wire-bonded to separated pins.

The LINAC uses use high energy electrons to produce X-rays with an energy spectrum ranging from 1MeV to 6MeV, and most probable energy is 2MeV. More information about the irradiation field and energy spectrum of this equipment can be found in [7]. The chip was placed inside a water equivalent phantom in order to simulate a radiotherapy charged particle equilibrium condition.

During the irradiation, the transistor back-gate, i.e. the backside of the SOI wafer, was biased with +12.4 V in order to improve the hole trapping in the BOX and improve the

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sensitivity to dose [8]. The other three terminals (drain, source and gate) of the front transistors were grounded. The irradiation was performed in incremental steps up to a dose of 20 Gy, at a dose rate of 4 Gy/min. After each step, the chip was removed from the phantom to measure drain currents versus back-gate voltages (I-V) curves of the devices. All measurements were taken at room temperature within 10 minutes from the end of the irradiation. I-V curves were measured sweeping the back-gate voltage while a +50 mV drain to source bias was applied. The front-gate was connected to the source terminal.

In a second experiment the dependence of the sensitivity to dose with the bias voltage was tested. This experiment consisted in irradiating another device in 5 Gy steps and for each step changing the bias voltage, starting from 0 V and ending with 20 V and 20 Gy.

III. RESULTS

Fig. 2 shows I-V curves of the devices before irradiation, after four 5 Gy irradiations, and after 3 days of annealing—at room temperature and with all terminals grounded. The devices showed a monotonic change in the threshold voltage with dose due to buildup of charge in the BOX. There is no significant change in the sub-threshold slope during the irradiation, which is an indication that the interface traps do not play a significant role on these transistors during irradiation.

However, after the three-day annealing, transistors PIP, NIN and NP1N showed a strong change in the I-V curve; exhibiting a stretchout in the subthreshold region and a shift towards more negative back-gate bias. On the other hand, I-V curves of PP1P, PP2P and PP12P devices were almost unmodified. The main difference between both groups is that the latter have high channel dopings, and turn on working in accumulation mode.

The stretchout of the I-V characteristics of PIP, NIN and NP1N devices during annealling would suggest an increase in interface traps density. However, the direction of change of V_T suggests an buildup of positive charge, which is not observed in most devices [8]. Another explanation could be the migration of ions—e.g. protons in the oxide [9].

Fig. 3 shows the variation of V_T as a function of dose and after irradiation. The change in the threshold voltage was measured as the change in the voltage for which the drain current is 1 nA. This simple method for ΔV_{th} extraction yielded similar results than the g_m/I_D method [10].

Fig. 4 shows the shift in V_{th} for back-gate transistors and their annealing. In this case they were irradiated in steps of 5 Gy while applying a back-gate bias voltage. This voltage was increased in each step up to 20 V as shown in the figure.

The first thing to notice in Fig. 4 is that the sensitivity is lower for 3 V bias. This effect could be due to a lower electric field (lower trapping yield) in the BOX, and this in turn due to depletion of the third interface as in Martino's potential drop model [11].

For bias voltages higher than 3 V the sensitivity is higher but it remains almost constant with bias. Both N and P bottom

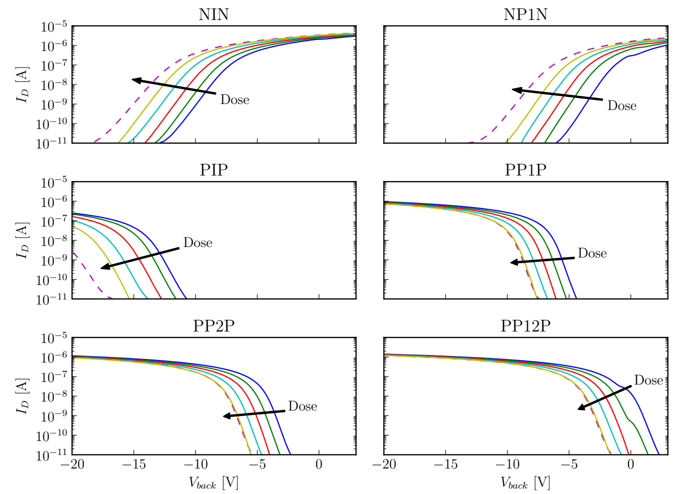

Fig. 2. Drain current versus back-gate voltage for doses of 0, 5, 10, 15 and 20 Gy. The dashed line corresponds to the measurement of the devices after 3 days of annealing on the desk. NP2N and NP12N were not functional and could not be measured.

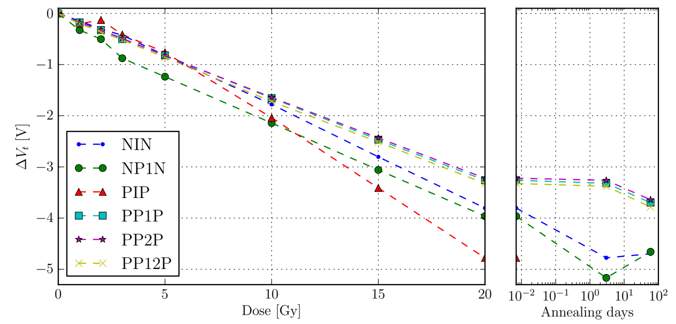

Fig. 3. Variation of the threshold voltage versus dose. Devices working in accumulation mode show better linearity than devices working in inversion mode. PIP device was out of the measurement range after the annealing period.

transistors have the same threshold voltage shift. Finally, there was around 15% recovery in the threshold voltage for an annealing period of 12 days on the shelf at room temperature.

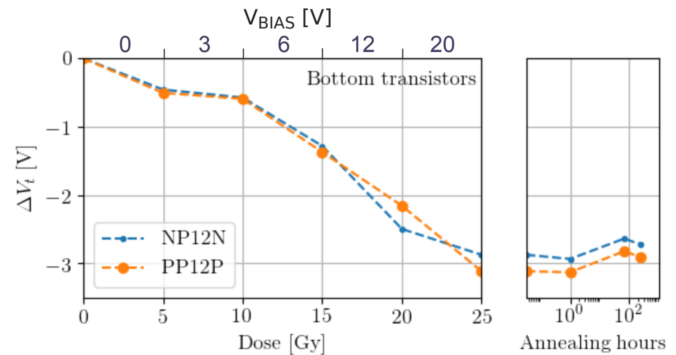

Fig. 4. Variation of the threshold voltage versus dose for irradiations with different bias voltages. The maximum obtained sensitivity is 191mV Gy^{-1} for PP12P with 20 V bias.

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IV. Discussion and Conclusions

The 400 nm thick BOX used in this work exhibit a sensitivity of 165 mV/Gy under 12.4 V bias. This sensitivity is higher than other similar devices used in dosimetry. For instance, the sensitivity of the 400 nm thick Field Oxide transistors presented in [12], was 40 mV/Gy under the same 12V gate bias. In [2] it was reported that 400 nm thick Tyndall dosimeters had approximately 100 mV/Gy under 5V gate bias. RFT 300 REM Oxford dosimeters [1] with 300nm thick gate oxide had a sensitivity of 125 mV/Gy under 9V gate bias—the same gate oxide field. Compared to other FD-SOI works which use BOX for dosimetry; [3] reported a sensitivity of 15mV/Gy with 5V gate bias on a 150nm thick BOX; [5] 12.5 mV/Gy on a 200 nm thick BOX manufactured by SOITEC, under zero volts bias; and Ref. [4] 1 mV/Gy with 145 nm BOX layer. The higher sensitivity observed in the devices of this work is not only caused by the thicker oxides, but also because a high hole capture probability. Assuming an electric field of $\simeq$ 0.3 MV/cm with a generation yield $\simeq$ 30% [8], and that the charge is captured very close to the Si-SiO_2 interface, the fraction of charge which remains trapped in the oxide is roughly a 95% of the available holes. This high trapping probability is consistent with the fact that BOX have a high oxygen vacancy defect concentration due to high temperature anneals during fabrication [5].

Finally, the high sensitivity of the BOX could be used for the development of a dosimeter with integrated reading electronics on the top side of the chip.

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