Ultralow Power Ionizing Dose Sensor Based on Complementary Fully Depleted MOS Transistors for Radiotherapy Application

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***Abstract*—We evaluate the use of thick buried oxide (BOX) of fully depleted silicon-on-insulator (FD-SOI) transistors for total ionizing dose (TID) measurements in a radiotherapy application. The devices were fabricated by a custom process at *Université Catholique de Leuven* (UCL) that allows one to make accumulation mode pMOS transistors and inversion mode nMOS transistors. We characterized the temperature behavior of these devices and the response under X-ray irradiation produced by an Elekta radiotherapy linear accelerator and compared the obtained dose sensitivity with other published works. Taking advantage of these devices, an ultralow power MOS ionizing dose sensor or MOS dosimeter with inherent temperature compensation is presented. This dosimeter achieved a sensitivity of 154 mV/Gy with a temperature error factor of 13 mGy/°C and a current consumption below 1 nA.**

***Index Terms*—Ionizing radiation sensors, silicon on insulator (SOI), silicon radiation detectors.**

I. INTRODUCTION

THE radiation-induced threshold voltage (V_T) shift of MOS transistors has been used for many years for the measurement of the Total Ionizing Dose (TID) [1]. To obtain devices with sensitivities useful for space and radiotherapy applications, the gate oxide thickness must be greater than several hundreds of nanometers, which is usually obtained in ad-hoc processes [2], [3]. In past years, there have been excellent publications about radiation effects in MOS oxides and devices [4], [5], even for silicon-on-insulator (SOI) devices [6]. Several works proposed the use in the dosimetry of transistors built using the buried oxide (BOX) available in SOI processes, using either the V_T shift in the back-gate transistor [7], [8] or the shift in front-gate transistors achieved through the body effect [9]. This work is an extension of [10], and is mainly focused on presenting and evaluating a new circuit that uses fully depleted silicon-on-insulator (FD-SOI) devices in a special arrangement to produce an output voltage proportional to the absorbed dose. The first part of the work deals with the characterization of single transistors against TID and temperature. This part serves as a presentation of devices and methods used in this work and gives an idea of the performance that can be achieved using single devices. In the second part, an ultralow power (ULP) circuit that can be used as an ionizing dose sensor, or a dosimeter, is presented along with an initial evaluation of its performance. We finalize this article with a discussion of the advantages of the ULP dosimeter when compared to single devices and the conclusions of this article.

II. DEVICES AND EXPERIMENTAL DETAILS

The FD-SOI MOS transistors used in this work, which are depicted in Fig. 1, were fabricated in the *Université Catholique de Leuven* (UCL) cleanroom using a heterogeneous fabrication process that was developed in-house [11], [12]. These transistors have a 31-nm-thick gate oxide, an 80-nm-thick layer of silicon, and a 400-nm-thick buried oxide (BOX), and are built on high-quality industrial-grade SmartCut UNIBOND wafers. The gate is n^+-poly and the channel is doped with Boron only, which leads to accumulation operating mode p-MOSFETs [13], [14] and inversion operating mode n-MOSFETs. Boron doping is divided into two lithography and implantation steps in such a way that it is possible to obtain four different channel dopings at low cost by masking only the desired areas. Blocking or masking both the implant steps yields a channel with an intrinsic Boron concentration of approximately 3×10^{14} cm^{-3} (I). Blocking either the first step

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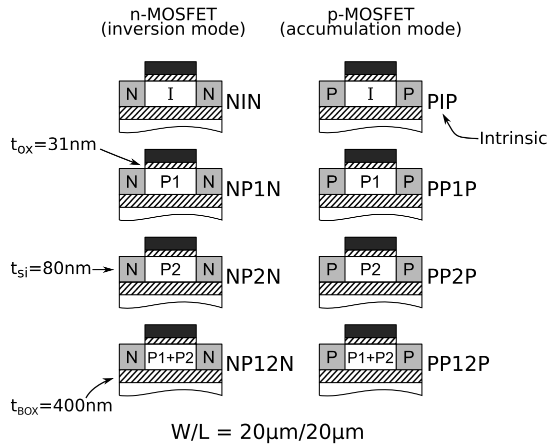

Fig. 1. FD-SOI MOS devices. The fabrication process allows different film dopings using two doping masks P1 and P2. Adapted from [11].

or the second one gives approximated channel concentrations of 2×10^{16} cm^{-3} and 3×10^{16} cm^{-3} (P1 and P2, respectively). Finally, allowing both implant steps on the same device gives a higher concentration of 5×10^{16} cm^{-3} (P12), which is the combination of both implants P1 and P2. Each implant gives a pair of threshold voltages for n- and p-MOS transistors that lead to quite symmetrical I–V curves.

A test chip was fabricated containing all types of transistors with channel lengths of 20 μm and widths of 20 μm. The die was encapsulated in a DIL24 ceramic package with an open lid and each transistor was wire-bonded to separated pins.

These devices were irradiated using an Elekta Synergy Linear Accelerator (LinAc) in a radiotherapy facility. This LinAc uses high-energy electrons to produce X-rays with an energy spectrum ranging from 1 to 6 MeV, and the most probable energy is 2 MeV. More information about the irradiation field and the energy spectrum of this equipment can be found in [15]. The chip was placed inside a water- equivalent phantom, in order to simulate the radiotherapy charged-particle equilibrium condition, on the central axis of the radiation beam and at the depth of the maximum dose. The LinAc field size was set to 10×10 cm^2 and the source-to-surface distance (SSD) was 100 cm. Throughout this article, all dose values will be given as the absorbed dose in water. A conversion to absorbed dose in silicon is straightforward.

During irradiation, the transistor back-gate, i.e., the backside of the SOI wafer, was biased with different voltages in order to analyze the dependence of hole trapping on bias. It has been reported that the hole trapping in the BOX can be improved this way, and so the sensitivity to the ionizing dose is improved [4]. The other three terminals (drain, source, and gate) of the front transistors were grounded. The irradiation was performed in incremental steps at a dose rate of 4 Gy/min. After each step, the chip was removed from the phantom and the drain currents versus the front-gate and back-gate voltages [$I_D(V_G)$ and $I_D(V_B)$ curves] were measured. All measurements were taken at room temperature within 10 min at the end of the irradiation. The I–V curves were measured by sweeping the front-gate voltage while $V_B = 0$ V and sweeping the back-gate voltage while $V_G = 0$ V. In all cases, the drain voltage was +50 mV and the source was grounded. Fig. 2 schematically

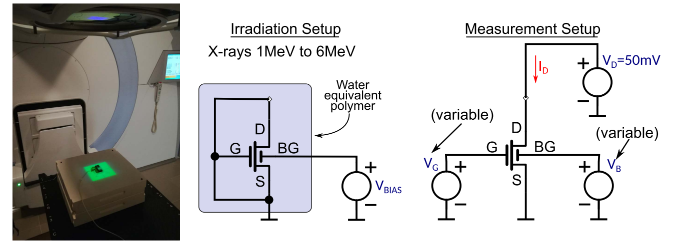

Fig. 2. Left: test chip placed in the radiotherapy facility. It was later covered with 13 cm of a water-equivalent polymer. Right: irradiation and measurement setups. For every measurement, the drain voltage was always 50 mV, whereas V_G was swept with V_B fixed at 0 V in order to measure the front-gate characteristic curve and V_B was swept with V_G fixed at 0 V to obtain the back-gate transistor characteristic curve.

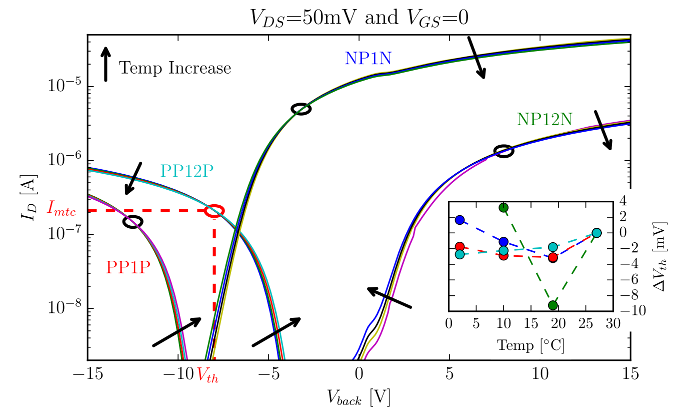

Fig. 3. Drain current versus back-gate voltage of four devices on the same die for 2, 10, 19, and 27 °C. The I_{mtc}–V_{th} points were marked with circles. The inset shows ΔV_{th} with respect to 27 °C. Using this method, the error introduced by temperature in the extraction of V_{th} is less than ±10 mV (for the given temperature range).

shows the irradiation and measurement setups. The drain currents were measured with a *Keithley 2450 SourceMeter* unit which, in its lowest current range (10 nA), has an accuracy of ±60 pA in the worst case.

The temperature dependence of the drain current versus the back-gate voltage was analyzed prior to the experiments. Fig. 3 shows the I–V curves of four devices in the same chip measured at 2 °C, 10 °C, 19 °C, and 27 °C. It can be seen that in the subthreshold region, the drain current increases with temperature following the inverse subthreshold slope usual dependence [16], whereas in inversion/accumulation, it decreases with temperature following the usual mobility dependence. In between those regions, there is an I_{mtc} current that is almost independent of temperature (mtc stands for "minimum temperature coefficient"). Usually, MOS dosimeters are biased with this current, and the voltage variation is taken as a measure of absorbed dose, independent of temperature. This method was used successfully before in [17] and [18].

In this work, the effective threshold voltage V_{th} of the devices was defined as the voltage for which the current is I_{mtc}, and this current was obtained prior to irradiation. The inset of Fig. 3 shows the change in the threshold voltage due to temperature when the devices are biased with the I_{mtc} current, and it can be seen that the voltage variation is less than ±10 mV in the measured temperature range. It is worth

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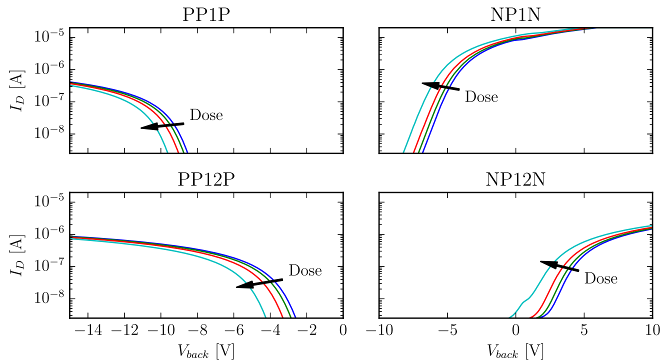

Fig. 4. Drain current versus back-gate voltage with the source and front-gate grounded, and 50 mV applied to the drain. Accumulated doses are 0, 10, 30, and 80 Gy.

noticing that the I_{mtc} point must be found for each device independently.

III. Evaluation of Single Transistors as Dosimeters

Single devices were tested with the aim of using them as radiation dosimeters for radiotherapy applications. Hence, the dependence of the threshold voltage on the absorbed dose was evaluated using the radiotherapy LinAc mentioned above.

Before the beginning of the experiment, the initial I–V curves were measured. Then, a single chip containing the devices was introduced in the water-equivalent polymer where it received a dose step of 5 Gy in approximately 1 min. Next, the chip was taken to the measurement setup, where the actual measurement of the devices began 3 min after the end of irradiation and took place for around 10 min. This process was repeated for the next 5, 10, 10, 25, and 25 Gy steps, which accounted for a total accumulated dose of 80 Gy. These irradiation steps were performed with all terminals grounded.

Fig. 4 shows the I–V curves of the devices, where some dose steps were skipped for clarity. The curves show a monotonic change in the threshold voltage with the accumulated dose due to the buildup of charge in the BOX. Also, there is no significant change in the subthreshold slope during irradiation, which is an indication that the interface traps do not play a significant role in the V_{th} shift of these transistors.

A. Threshold Voltage Shift Under 0 V Bias

Fig. 5 shows the V_{th} shift as a function of accumulated dose and its recovery after the experiment due to annealing. This figure corresponds to the same chip of Fig. 4 that was irradiated under 0 V bias, i.e., with all terminals grounded. The effective threshold voltages of interest for this work were extracted from the I_{mtc} point of the I–V curves.

The sensitivity of the back-gate transistors (BGTs)—transistors formed by the back-substrate, the BOX, and the Si film—is higher than that of the front-gate transistors (FGTs). This is expected and can be explained by the Lim–Fossum model of the inversion-mode FD-SOI transistors [19] and by the Flandre-Terao model for accumulation-mode transistors [14], by introducing a fixed charge in the BOX, although some front-gate oxide charge is also needed to account for the total shift. Therefore, FGTs are less sensitive to radiation, resulting

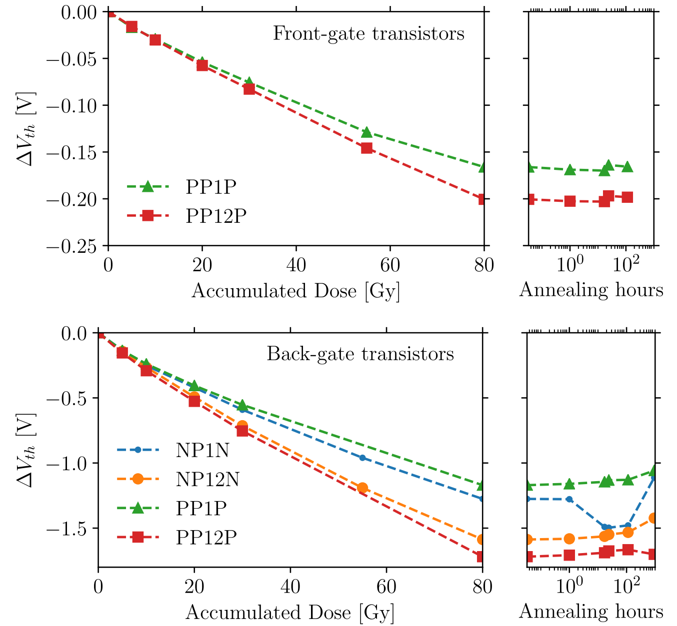

Fig. 5. Variation of the threshold voltage versus accumulated dose for successive irradiation with 0-V back-gate bias, followed by an annealing period. The dose steps were: 5, 5, 10, 10, 25, and 25 Gy.

in a variation of the threshold voltage of FGTs ΔV_{tf} being around 10% of that of BGTs ΔV_{tb}, and this is related to the ratio of gate oxide and BOX thicknesses.

Also, devices with higher channel doping seem to be more sensitive to radiation, as seen in Fig. 5, where ΔV_{th} for the P12 doping profile is higher than that for P1. This could be explained as a stronger electric field in the BOX, which increases the trapping yield [4]. Also, devices with higher doping have a more linear response to dose.

The annealing was performed at room temperature between 18 °C and 24 °C, and with all terminals grounded. The devices presented a 10%–12% reduction in ΔV_{tb} after one month.

B. Threshold Voltage Shift for Different Bias Conditions

Another chip was irradiated in the radiotherapy facility and the procedure was analogous to what was described previously. The only difference was that this time the back-gate was biased to increasing voltages, from 0 to 20 V, during each irradiation step, while the remaining terminals were grounded. In all steps, the dose was 5 Gy. The first irradiation step was performed with a back-gate bias of 0 V, the second step with 3 V, the third one with 6 V, and so on with 12 and 20 V applied to the back-gate. In-between steps, the I–V curves of the devices were measured as described before.

Fig. 6 shows the V_{th} shift of the front- and back-gate transistors and their annealing. The first thing to notice is that the sensitivity is lower for 3 V bias. This effect could be due to a lower electric field (lower trapping yield) in the BOX, and this, in turn, is due to depletion of the third interface as in Martino's potential drop model [20].

For bias voltages higher than 3 V, the sensitivity is higher, but it remains almost constant with bias. Although a higher electric field implies a higher charge yield, i.e., the fraction of holes that escapes initial recombination, it also implies a

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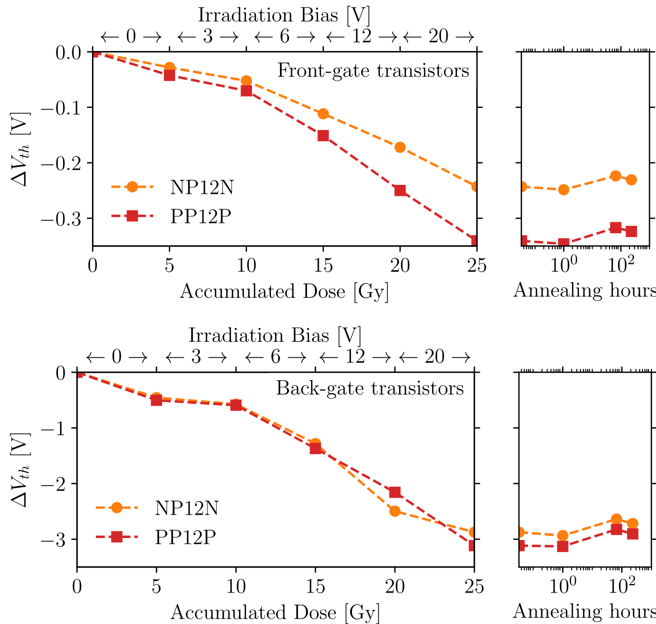

Fig. 6. Variation of the threshold voltage versus accumulated dose for successive 5 Gy irradiation, each one with an applied back-gate bias voltage shown by the top arrows, followed by an annealing period. The maximum obtained sensitivity is 191 mV Gy^{-1} for BGT PP12P with 20-V bias.

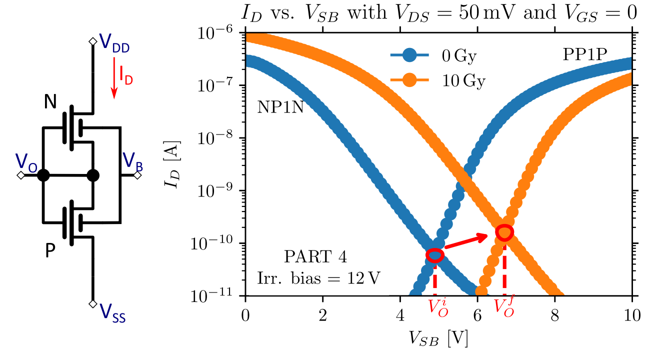

Fig. 7. Left: proposed ULP dosimeter. Right: drain current versus source back-gate voltage of NP1N and PP1P transistors. For $V_B = 0$ V, the voltage at the crossing point of the nMOS and pMOS curves is the output voltage of the ULP dosimeter.

reduction in the hole trapping cross section near the interface, as was reported in [21]. Therefore, there is a saturation for electric fields in the range 0.2–1 MV.cm^{-1}.

Finally, the annealing was performed under the same conditions as before, obtaining a recovery of the threshold voltage below 15% after 120 h.

IV. Ultralow Power MOS Dosimeter

In this section, we present a ULP dosimeter using FD-SOI devices, which is based on the ULP voltage reference published in [22]. This dosimeter uses two transistors connected as seen in Fig. 7. The drains of the n- and p-MOSFETs are connected to V_{DD} and V_{SS}, respectively, while their sources are short-circuited with their gates and connected together to form the output node V_{O}. Using V_{SS} as the reference voltage, V_{DD} must be biased positive at a voltage greater than the equilibrium voltage of V_{O}, which depends on the back-gate voltage V_{B}. As both transistors are fabricated on the same handling wafer, the back-gate is the same for both devices. Fig. 7 also shows in a single plot the I_{D}–V_{SB} curves of NP1N and PP1P devices before and after 10 Gy. It is worth noticing that in the case of V_{S} being equal to 0 V, the x-axis is the same as in Fig. 4, but reversed.

Since the devices are in series in the ULP dosimeter, the same amount of current must flow through both channels. Also, both devices have their front-gates connected to their sources, making $V_{gs}^N = V_{gs}^P = 0$ V. To satisfy these two conditions, the voltage V_{O} must settle at the intercept point of the I_{D}–V_{SB} curves of the n- and p-transistors, shown with red circles in Fig. 7, i.e., around 5 V with $V_{\text{B}} = 0$ before irradiation. The drain current at this point is below 0.1 nA and, hence, the power dissipation is less than 1 nW.

When the devices are exposed to ionizing radiation, the I–V curves that were shifted to the left in the plots of Fig. 4 are now shifted to the right in Fig. 7 (due to the change of reference from source to back-gate), increasing the output voltage of the ULP dosimeter. According to Levacq's equations [23] and since the subthreshold slope shift with dose is negligible, V_{O} will be increased by the same magnitude as the V_{th} shift, making the output voltage proportional to the absorbed radiation dose. Also, since both devices can be placed next to each other, with the exact same size and an almost equal doping profile, the threshold voltage shift with dose will match very well. This means that, in principle, the curves of n- and p-transistors of Fig. 7 will shift by the same amount, and the current at the crossing point of N and P will not change. However, the plot shows a slight increase in the current that can be attributed to the small difference in the threshold voltage shift of n- and p-MOSFETs, as is seen in Fig. 5.

The circuit is also stabilized against temperature. As shown in [22], an increase in temperature will increase the current consumption exponentially due to the increase in thermally generated carriers in the subthreshold region. But again, since both devices are equally doped, the increase will be almost equal for both and ideally there would not be any voltage shift of the equilibrium point, mitigating temperature-induced output voltage variations.

A. Experimental Verification of the ULP MOS Dosimeter

The sensor built with a pair of n- and p-transistors on the same die was irradiated using the same irradiation setup as in Fig. 2. After irradiation, the devices were connected as in the ULP dosimeter circuit of Fig. 7 and the output voltage and the current consumption were measured. For this experiment, devices with the highest doping profiles were used (NP12N and PP12P), as they have shown the best sensitivity in Section III.

The experiment was carried out in two different campaigns: In the first one, the chip was irradiated under 0 V bias and the ULP dosimeter measurements were done with $V_{\text{B}} = 0$ V. The ionizing dose was delivered in 5 Gy steps up to 25 Gy. The procedure was the same as explained in Section III: after

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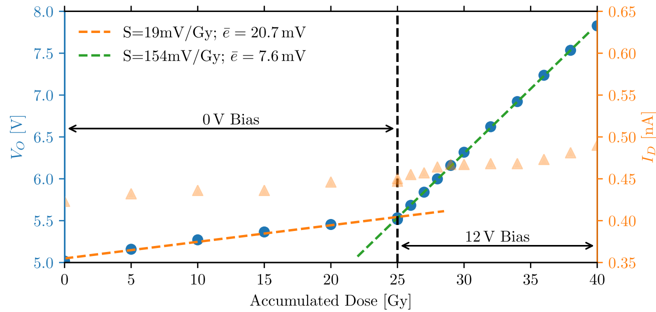

Fig. 8. Experimental results of the ULP dosimeter: equilibrium voltage V_O and bias current I_D measured at $V_\mathrm{DD} = 8$ V, $V_\mathrm{B} = 0$ V and $V_\mathrm{SS} = 0$ V. The devices were irradiated in two different campaigns under back-gate biases equal to 0 and 12 V, using the same irradiation setup as in Fig. 2. In-between campaigns, there was an annealing period of 20 days in which a recovery of 0.5% was measured.

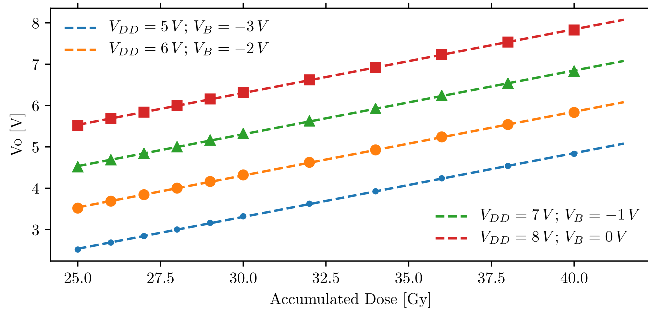

Fig. 9. Measurements during the second campaign for different back-gate voltages and maintaining a voltage difference of 8 V between V_DD and V_B. The sensitivity is equal to 154 mV/Gy in all cases.

each irradiation step, the chip was taken to the measurement setup and the output voltage was read approximately 2 min after exposure.

In the second campaign, the same chip was used and the procedure was similar, but this time the irradiation was performed with 12 V applied to the back-gate, and the output voltage was measured at different back-gate voltages V_B. In-between campaigns, the devices were kept at room temperature with all terminals grounded. A slight recovery was observed, but it was below 0.5% of the V_O nominal value.

Fig. 8 shows the results of both campaigns, where data points were fit with a linear regression using the least-squares method. The deviation of the data points with respect to the linear fit is given by the $\bar{e}$ parameter, which was calculated as the mean absolute error. The plot shows that the circuit behaves as expected, i.e., increases the output voltage with the absorbed dose, and that applying a bias voltage during irradiation increases the sensitivity in the same way as in Section III. Linearity was much better for irradiation under 12 V bias than for 0 V bias, as shown by the mean errors $\bar{e}$. Finally, there is a slight increase in the current consumption that can be attributed to the difference in the threshold voltage shifts of n- and p-devices.

Fig. 9 shows measurements of the second campaign at different back-gate voltages. The only effect of changing V_B is shifting the output voltage by the same amount, but V_DD must be changed accordingly to keep the two MOSFETs saturated.

The temperature dependence of the output voltage was measured prior to irradiation and is shown in Fig. 10. It can be seen that the output voltage decreases by 2 mV/°C, while the current consumption increases exponentially as expected.

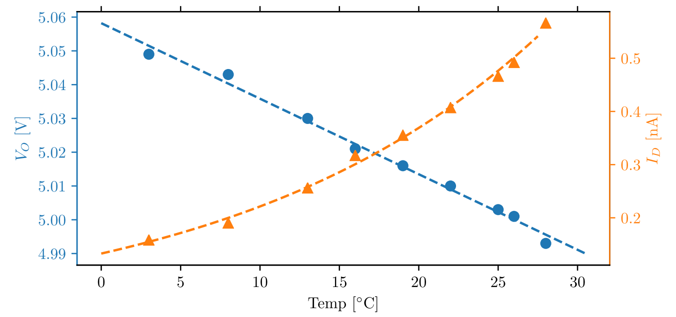

Fig. 10. Temperature characterization of the ULP dosimeter. V_O varies linearly with slope equal to −2 mV/°C, while I_D increases exponentially with temperature.

The *temperature error factor* (TEF) is defined as the ratio between the sensitivity to dose and the sensitivity to temperature, and it gives the error in dose measurement per unit of temperature change [24]. For a sensitivity of 154 mV/Gy (Fig. 9), the TEF of the ULP dosimeter is 13 mGy/°C.

V. Discussion

In Sections III-B and IV-A, a bias voltage was applied to the back-gate, so it is worth mentioning that no back-gate bias instabilities were observed before or after irradiation for electric fields (up to 0.5 MV.cm^{-1}) and stressing times (up to 300 s) used in this work. Such an effect has been reported to have occurred at high temperatures [25] or for substrates that received a special treatment, like annealing in a forming gas atmosphere [26], or silicon implantation [27], while we use here the highest-quality recent SOI wafers. Although the primary application here is external beam radiotherapy, it is worth mentioning what to expect when irradiating single devices or the ULP dosimeter with other dose rates and other energies. With respect to the dose rate, it has been shown that generally the response of MOS oxides to radiation can show "apparent" dose rate effects, but it is commonly accepted that there are no true effects [4], [5], even for dose rates whose orders of magnitude were different. This means that for lower or higher dose rates than the one used in this work, the measured ΔV_th immediately after irradiation will be different, but if the time elapsed between the beginning of irradiation and the ΔV_th measurement is the same, then the final ΔV_th will be equal, regardless of what dose rate is used, at least to the first order. Therefore, in the specific case of radiotherapy with Megavoltage LinAcs, in which the average dose rate does not change significantly—it is fixed around 1 Gy.min^{-1} for radiobiological reasons [28]—the response of the devices will be quite the same for different dose rates.

Also, it has been shown [29], [30] that by using the linear systems theory and carefully modeling the impulse response of devices to a short radiation pulse, it is generally possible to predict the response of devices to different dose rates—except when the response is nonlinear with dose. Since a Megavoltage LinAc delivers the dose as a train of high dose rate and short width radiation pulses ($\approx 2\ \mu$s), which are ms apart, the application of this theory is viable, in principle.

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For photon energies different than the ones used in this work, the studies of MOS oxides ([4], [5]) have shown that the only difference is the fractional yield, i.e., the fraction of initial charge that escapes recombination. For higher energy photons, the fractional yield will be higher and for lower energy photons, the fractional yield will be lower. The initial recombination might show other behavior when using particles other than photons. For example, highly ionizing particles tend to produce lower fractional yields. Therefore, the response of single devices and the response of the ULP dosimeter will change accordingly. The limit to this behavior is generally for photon energies below 100 keV, when the interaction of radiation with the package material starts to modify the dosimeter response [31]. But this limit energy is much lower than the range generally used with Megavoltage LinAcs.

In Sections V-A and B, comparisons between single devices and other MOS dosimeters and single devices versus the ULP dosimeter are presented. The sensitivity to the ionizing radiation dose is compared and also the TEF.

A. Single Devices versus Other MOS Dosimeters

The 400-nm-thick BOX used in this work exhibits a sensitivity of 165 mV/Gy under 12.4 V bias. This sensitivity is higher than other similar devices used in dosimetry. For instance, the sensitivity of the 400-nm-thick field oxide transistors presented in [32] was 40 mV/Gy under the same 12 V gate bias. In [3], it was reported that 400-nm-thick Tyndall dosimeters had approximately 100 mV/Gy under 5 V gate bias. RFT 300 REM Oxford dosimeters [2] with a 300-nm-thick gate oxide had a sensitivity of 125 mV/Gy under 9 V gate bias—the same gate oxide field. Compared to other FD-SOI works which use BOX for dosimetry, [7] reported a sensitivity of 15 mV/Gy with 5 V gate bias on a 150-nm-thick BOX; [9] 12.5 mV/Gy on a 200-nm-thick BOX manufactured by SOITEC, under zero volt bias; and [8] 1 mV/Gy with a 145-nm BOX layer.

The higher sensitivity observed in the devices of this work is not only caused by the thicker oxides, but also because of a high hole capture probability. Assuming an electric field of $\simeq$ 0.3 MV/cm with a generation yield $\simeq$ 30% [4], and that the charge is captured very close to the Si–SiO_2 interface, the fraction of charge which remains trapped in the oxide is roughly 95% of the available holes. This high trapping probability is consistent with the fact that BOX has a high oxygen vacancy defect concentration due to high temperature annealing during fabrication [9].

Another important parameter for a dosimeter is the fading due to neutralization of trapped charges. For the FD-SOI devices in [9] Shaneyfelt *et al.* observed a recuperation of less than 10% in the threshold voltage shift for their BOX RadFETs during a period of 700 h; on the other hand, in [8], the retention of the charge lasted up to 90 days without considerable fading. The devices of this work showed a fading of charge, or recovery of the threshold voltage, of around 10% in a period of 100 h after irradiation. Since the radiation response is related to the processing and history of the oxide in particular [5], there is no significant difference between the three works, at least for the periods of time analyzed.

B. Single Devices Versus the ULP Dosimeter Circuit

The sensitivity obtained with single devices and the ULP dosimeter is roughly the same ($\approx$ 160 mV/Gy at 12 V bias), and this is expected because the ULP dosimeter is an arrangement of two single devices with the same dimensions, doping profiles, and oxide thicknesses. In principle, charge trapping in the BOX produces a shift in the threshold voltages that has the same magnitude and sign in both devices. This V_{th} shift is also affected by the interface charge density which adds to the oxide charge-induced shift, but with different signs for n- and p-MOSFETs. During the characterization of single devices, it has not been seen that the interface charge played a significant role in the BGTs, especially when irradiated with a high back-gate bias voltage. If there was such an effect, then the difference introduced in the shift of the I–V curves of n- and p-devices would be reflected in a strong increase of the current consumption of the ULP dosimeter with accumulated dose.

Regarding the temperature, the ULP dosimeter has an intrinsic temperature shift rejection, which mostly depends on the device mismatch. On the other hand, it has been proven that the V_{th} extraction using the I_{mtc} current is dose dependent [33], and so the main source of inaccuracy when using single MOS devices as dosimeters. The TEF obtained with the ULP dosimeter in this work (13 mGy/°C) is lower than the one reported in [33] (20 mGy/°C) by using only the I_{mtc} method, but is higher than the one reported in the same work using a reduced temperature range (6 mGy/°C), and is also higher than the TEF obtained with differential circuits in [24] (0.7 mGy/°C) and [34] (5.9 mGy/°C).

The mismatch between devices plays an important role in the sensitivity and power consumption of the ULP dosimeter. So it is important to note that in this work the n- and p-devices were laid out on the same substrate, but separated from each other. Therefore, the mismatch could be reduced by using layout matching techniques, such as common centroid and the addition of dummy devices. It is also possible to adapt the W/L ratio of transistors in order to reduce the temperature sensitivity of the output voltage, as demonstrated in [35].

Finally, the ULP dosimeter circuit requires no power during irradiation and its power consumption is below 0.1 nW during readout. For example, a typical RadFET [2] or FoxFET [32] is read out with currents on the order of hundreds of microamperes and voltages from one to tens of volts, consuming power in the μW range in the best case. Another CMOS-based ULP dosimeter described in [36] has a power consumption of 1 μW, which is at least three orders of magnitude more than the ULP circuit presented here.

VI. Conclusion

Characterization of the FD-SOI MOS transistors fabricated by the process developed at UCL has been presented. It has been shown that these devices are suitable for MOS dosimetry due to their 400-nm-thick BOX and their high sensitivity to

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dose, up to 191 mV/Gy under a back-gate bias of 20 V. It has also been shown that the sensitivity to ionizing radiation can be improved by applying a bias voltage to the back-gate of the devices during irradiation and by using the devices with the highest doping profiles.

Moreover, the high sensitivity to the dose of the BOX and the low threshold voltage shift of the FGTs can be used for the development of a dosimeter with integrated read-out electronics on the top side of the chip.

In this last direction, we presented an ULP dosimeter made of only one n-MOSFET and one p-MOSFET working in the subthreshold regime and with intrinsic temperature compensation. This is a small circuit that can be connected to amplifiers or signal-conditioning circuits directly fabricated on the same thin silicon film. The ULP dosimeter has the same sensitivity as single devices, but it has the advantage of a reduced TEF (13 mGy/°C @ 12 V bias), which could be reduced even more with a careful design of the sensor, i.e., using layout matching techniques and adjusting the W/L ratio of n- and p-devices.

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