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A TEMPERATURE COMPENSATED SINGLE CHANNEL ANALYZER FOR MONITORING PURPOSES

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The design of a single channel analyzer to be used as a monitor of reactor fission products is presented. Emphasis is placed on reliability through circuit simplification and minimum number of components compatible with an acceptable level of accuracy. The circuit comprises six integrated circuits and associated discrete components. Integral and differential nonlinearity attainable with an elementary window discriminator are evaluated, and conditions for its proper triggering are discussed. The temperature behaviour of a TTL driven counting rate meter is shown to be independent of the counting rate and of the design of the array of diode pumps. The temperature compensation required for this section is calculated and implemented using a simple circuit arrangement.

1. Introduction

The design of instruments for monitoring purposes is based on entirely different requirements from those which apply to laboratory instruments performing the same kind of measurements. In the latter, accuracy would never be sacrificed for a reasonable level of circuit complexity while in the former, the stringent requirements of reliability and/or portability pose the compromise between the minimum number of circuit components compatible with a tolerable level of accuracy.

In the case of single channel analyzers, a laboratory instrument requires very stable, uniform and small window widths in order to obtain accurate spectra. A monitoring SCA, on the other hand, must reliably report counting rates at energy windows that comprise well known peaks and that need not be smaller than a few percent of the total energy range. Regarding minimization of the number of circuit components, the use of integrated circuits is of invaluable help. In SCA's however, a number of non-integrated components is unavoidable, e.g. capacitors, diodes and resistors for the pumps of the counting rate meter, precision potentiometers to set the energy levels, capacitors for filtering and timing purposes, etc. What can be done is a careful selection of the available integrated circuits so that full advantage is taken of the characteristics and/or the internal organization of each IC while the minimum number of non-integrated components results from a particular choice.

The single channel analyzer presented here has been designed to be used as a monitor of fission products present in the water cooling circuit of the RA-3 reactor. Each of several SCA's will monitor an energy window of interest and will provide a signal to a trip circuit. Reliability has therefore been a major design consideration.

The circuit comprises six IC's and the mentioned non-integrated components. Two linear IC's are used as lower- and upper level comparators of the input signal amplitude. Two digital IC's are used for the triggering section, one provides two monostable multivibrators as required by the timing scheme adopted and the other performs the anticoincidence and directly charges the diode pump circuits. The fifth IC is a linear amplifier which adds the pumps' currents to provide an output signal. The sixth IC is a linear amplifier which together with some discrete components provides the supply voltage for the mentioned digital IC's, the scale calibration and the temperature compensation as required by the counting rate meter.

2. Circuit description

2.1. Input section

Differential comparators of the type μA710 have been applied as lower- and upper level comparators of the input signal amplitude, due to their suitable characteristics (temperature stability, low input offset voltage, input range). The comparison voltage for the reference input of the comparators (IC1 and IC2, see fig. 1) is obtained from two 10-turn precision potentiometers. Both potentiometers (P1 for the lower- and P2 for the upper threshold settings) are connected in parallel and fed from a stable supply.

Controlling the lower- and upper threshold settings (instead of e.g. the lower threshold and the window width) has the following disadvantages:

a) The inherent nonlinearity of P1 and P2 (0.15%

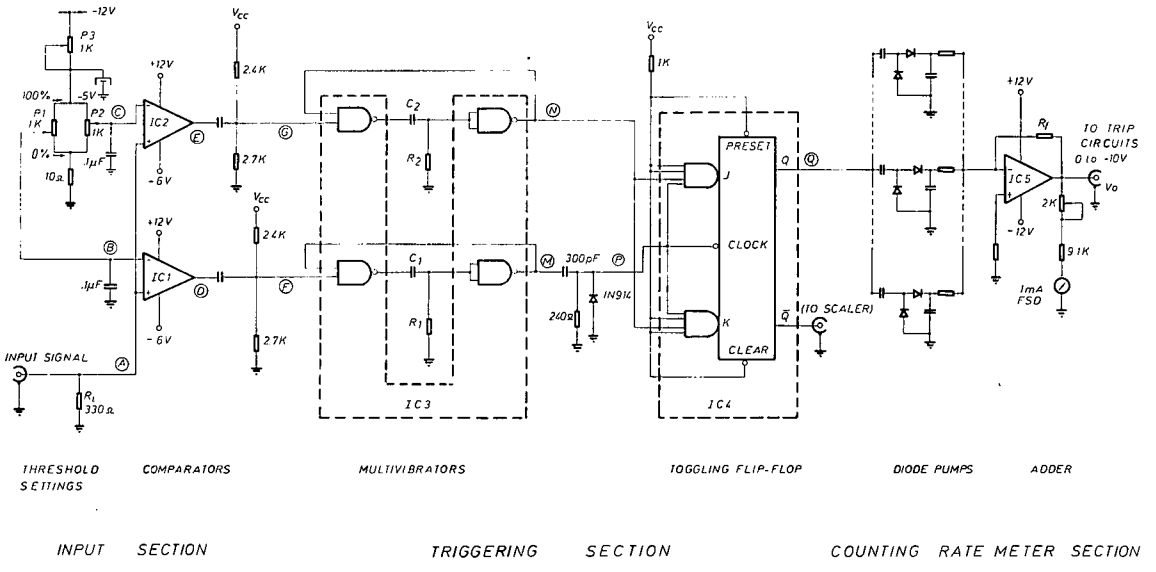


Fig. 1. Circuit of single channel analyzer. IC1 and IC2 = μA710, IC3 = SN7400, IC4 = SN7472 and IC5 = MC1456G.

in commercially available precision potentiometers) adds up algebraically and the differential nonlinearity may increase enormously as the window width decreases below of about 3%.

b) Both potentiometers' shafts have to be rotated simultaneously if the window width is to be kept constant when moving it along the energy spectrum.

Both disadvantages do not apply to a monitoring instrument; neither too small window widths nor a sliding window are required. On the other hand, controlling the lower and upper thresholds presents advantages which result in the following circuit simplifications and improved reliability:

1) No need exists for a floating voltage supply (as would be the case if the window width were a variable setting). Both potentiometers can be connected in parallel and fed from the same supply. This in turn avoids the need for limiters to protect the reference input of the comparators with respect to their stated input voltage range.

2) Further circuit simplification is possible due to the parallel connection of P1 and P2. In the published design of a window discriminator[1]), emitter followers are inserted between the signal and reference sources and the respective comparators' inputs. In this way the contribution to integral nonlinearity introduced by the nonzero input bias current of a comparator flowing through nonequal signal and reference source resistances is considerably decreased (a minimum signal input resistance of 1 kΩ and the same comparator types have been applied).

Due to the parallel connection of P1 and P2 and to the resistance values chosen, the insertion of the mentioned emitter followers could be avoided. The signal and reference sources are directly connected to the respective comparators' inputs, as shown in fig. 1. The resulting worst case integral nonlinearity introduced by the input bias current of a comparator can be calculated as

$$\Delta V_{b_{max}} = \Delta R_{max} I_{b_{max}}, \quad (1)$$

with

$$\Delta R = R_{ref} - R_{sig}, \quad (2)$$

where R_{ref} and R_{sig} are the reference and signal source resistances as seen from the comparators' inputs, and $I_{b_{max}}$ is the maximum input bias current of the applied comparator types ($I_{b_{max}} = 20\ \mu A$). It follows from the input section of the circuit of fig. 1 that the maximum value of ΔR occurs at the 0% setting of either P1 or P2. The resulting value is $\Delta V_{b_{max}} = -6.4$ mV or -0.13% of the input voltage range of 5 V. This value decreases to within $\pm 0.02\%$ in the upper 70% of the scale of settings.

3) No need exists for a switch to operate the SCA in the discriminator mode. To do this it is just sufficient to set P2 at its 100% position.

2.2. Triggering section

In the following, a negative polarity and a maximum amplitude of −5 V are assumed for the input signal (two additional inverters would be needed for positive

polarity, but the circuit of fig. 1 is easily adaptable). No assumptions are made about the shape or duration of the input pulse other than a minimum time to peak of about 100 ns, as required by the comparators. The triggering method applied is explained with the timing diagram of fig. 2. The output of each comparator is differentiated to effectively trigger the monostable multivibrator that follows it. Each multivibrator is built using two two-input NAND gates (from IC3, a quad two-input NAND gates SN7400) and two passive components[2]). The positive going trailing edge of the multivibrator following the lower level comparator is differentiated and used as the clock input of a toggle-connected flip-flop (IC4, a J-K flip-flop SN7472). The toggling action of this pulse is inhibited at the J and K inputs of the flip-flop if the multivibrator following the upper level comparator has been triggered. In this way, only those pulses comprised within the window will change the state of the flip-flop outputs.

In order to ensure proper triggering at any threshold settings, the following condition must be met

$$t_p < T_1 < T_2, \qquad (3)$$

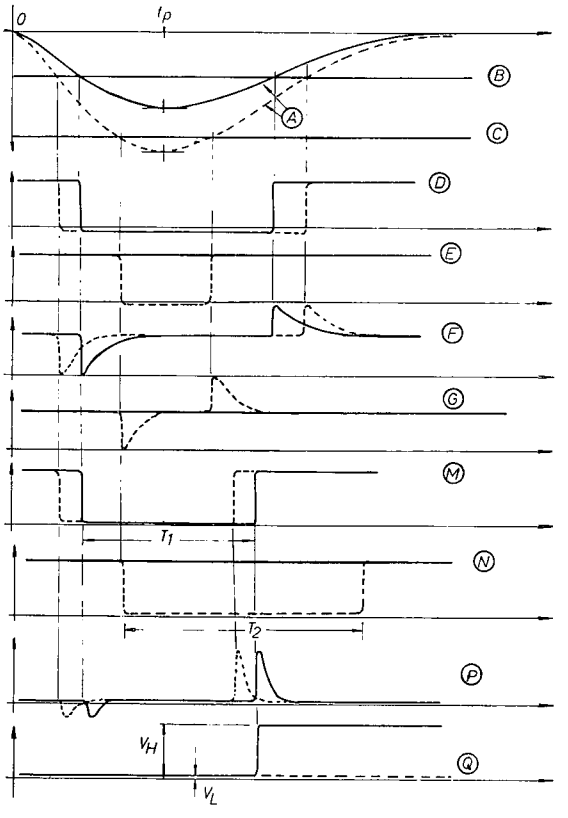


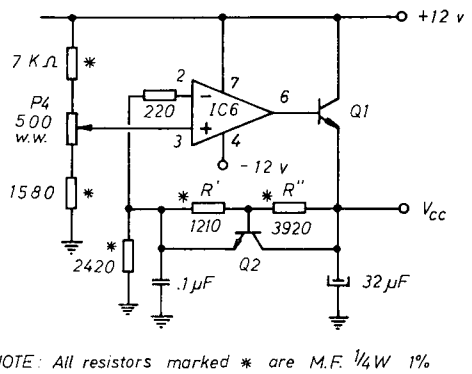
Fig. 2. Timing diagram. Circled letters refer to fig. 1.

where t_p is the time to peak of the input signal and T_1 and T_2 are the durations of the multivibrators' pulses following the lower- and upper level comparators, respectively (which are determined by R_1 and C_1 and by R_2 and C_2). A compromise must be found for the durations of T_1 and T_2, because if condition (3) is met too amply the dead time of the instrument is unnecessarily long and if it is met too tightly improper triggering may occur due to the limited duty cycle of the multivibrators. The high output current capability of TTL was the main reason of the choice for IC4. This permits a direct connection of one of the flip-flop outputs (Q) to the input of the diode pumps. The other flip-flop output ($\bar{Q}$) may be used to send pulses to a scaler, in which case the scaler's counts or its counting time must be doubled because a full output pulse corresponds to two input pulses.

2.3. Counting rate meter section

A high input impedance differential amplifier (IC5) is used to add the output currents of the diode pumps and to provide a 0 to -10 V signal to the trip circuit to which this instrument is connected.

Calibration of the counting rate meter to correspond to a predetermined scale (e.g. 2 V/decade) could be done by means of a potentiometer in the feedback loop of IC5 but this is not a convenient method due to the high impedance of the loop. A more indirect calibration method has been preferred. As can be shown using eqs. (11), (14) and (26) of appendix 1, a relative variation in the TTL supply voltage produces an equal relative variation on the output voltage V_0 of the rate meter provided that the counting rate and the ambient temperature are kept constant. Adjustment of V_{cc} at 25 °C between 4.67 V and 5.33 V [so that this



NOTE: All resistors marked * are M.F. 1/4 W 1%

Fig. 3. Adjustable, temperature dependent voltage source providing the supply for IC3 and IC4 and the calibration and the temperature compensation for the counting rate meter section. IC6 = μA741, Q1 = 2N697 and Q2 = MPS2923.

adjustment and the temperature compensation circuit described later do not exceed the 4.50 V $\leq V_{cc} \leq$ 5.50 V limits[3]) of supply voltage] by means of potentiometer P4 of fig. 3 allows a range of more than 13% for the calibration of the V_0 versus log n characteristic of the counting rate meter.

3. Temperature behaviour of the discriminator

Temperature dependence of the threshold settings and of the window width was measured for the 30%–35%, 60%–65% and 90%–95% lower-upper settings using an Ortec 448 precision pulser. The input and the triggering sections of the circuit of fig. 1 were placed in a thermal chamber for this purpose.

Variations of less than 0.1% were measured in the lower and upper threshold levels in the 0°C to 50°C temperature range. These variations tended to track each other, so that window width variations were almost negligible, a value of only 0.4% having been measured (i.e. a 1 mV variation in the difference between upper and lower thresholds of a 250 mV or 5% window width) in the mentioned temperature range.

4. Temperature behaviour of the counting rate meter

The circuit of fig. 4 was placed in the thermal chamber in order to measure the degree of stability of the output voltage V_0 with respect to ambient temperature variations between 0°C and 50°C. The supply voltage for IC4 during this test was provided by a stable source external to the thermal chamber. Use was made of an array of five diode pumps designed to cover the counting rates ranging from 1 to 10^4 counts/s. Low reverse current diode types 1N137A and load resistors of 3.9 MΩ were applied for the pumps.

The measurements showed that the relative rate of change of V_0 with respect to temperature was almost independent of the counting rate and almost constant within the mentioned temperature range. The values obtained ranged from 0.33%/°C to 0.35%/°C. These results are explained in appendix 1.

5. Temperature compensation of the counting rate meter

The relative variation of V_0 over the whole temperature range is, using the calculated value of eq. (26) of appendix 1, 0.342%/°C (50°C − 0°C) = 17.2%. This indicates the need to compensate the circuit of the rate meter with respect to ambient temperature variations. A method that has been found suitable to achieve this compensation is to make the supply voltage V_{cc} of the digital IC's (IC3 and IC4) temperature dependent. The rate of change of V_{cc} with temperature necessary to cancel temperature induced variations of the output voltage of the rate meter is calculated in appendix 2 and is

$$\frac{dV_{cc}}{dT} = -8.72 \text{ mV/°C}. \tag{4}$$

Since the temperature behaviour of the counting rate meter is fully due to silicon components (IC4, D1 and D2, see appendix 1), these are preferable to perform the temperature compensation. The circuit of fig. 3 provides a voltage that decreases with temperature with good approximation to the requirement of eq. (4). The arrangement in the feedback loop of IC6 (Q2, R′ and R″ of fig. 3) effectively simulates the current–voltage characteristic and the temperature behaviour of any* desired number of series-connected, forward-biased diodes[4]). The number of diodes is approximately given by the relationship

$$d = \frac{R''}{R'} + 1, \tag{5}$$

which results from supposing zero base current in Q2 and from comparing the collector–base to the base–emitter (= 1 diode) voltage drops of Q2 expressed in terms of resistors R″ and R′ respectively. The values of these resistors are further determined by the current that can flow through them, which should be neither smaller than about 10 times the (actually nonzero) base current of Q2 nor larger than the collector current

* Provisions must be taken if this number reaches the order of magnitude of the dc current gain of Q2.

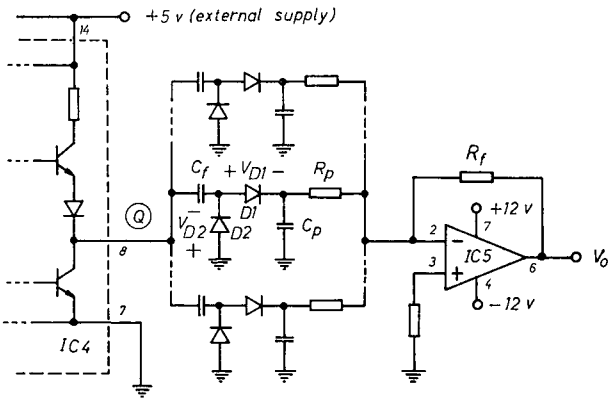


Fig. 4. Circuit for the analysis of the temperature behaviour of the counting rate meter section. D1 and D2 of all pumps are 1N137A.

of Q2. The number of diodes to be simulated by the arrangement in the feedback loop of IC6 is

$$d = \frac{dV_{cc}/dT}{dV_{BE}/dT}, \tag{6}$$

where V_{BE} is the base–emitter voltage drop of Q2 at a collector current of about 0.5 mA (imposed by the resistors of the circuit of fig. 3) and at $T = 25\,°C$. Under these conditions, $V_{BE} = 0.6$ V for the transistor type applied for Q2. Application of eq. (17) of appendix 1 using this value yields

$$\frac{dV_{BE}}{dT} = -2.03\ \text{mV/°C}. \tag{7}$$

Using the numerical values of eqs. (4) and (7) into eq. (6), the number of diodes to be simulated is $d = 4.3$. This result, the above considerations and use of eq. (5) explain the values chosen for R′ and R″ of fig. 3.

Measurements in the thermal chamber showed that when the circuit of fig. 3 was used to supply the V_{cc} voltage for the TTL IC's, ambient temperatures ranging from 0 °C to 50 °C produced relative variations of V_0 smaller than 0.6%.

6. Construction

The circuits of figs. 1 and 3, including the mentioned array of diode pumps, together with the preamplifier and amplifier stages preceding the SCA (not mentioned in this article) have been built on a 17.5 cm by 19 cm single sided fiberglass printed circuit plate and placed in a single width NIM module.

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Appendix 1

Calculation of the relative rate of change of V_0 with respect to temperature.

Since V_0 is the sum of output pump voltages, temperature induced variations of the output voltage V_p of an individual pump will be discussed first (see fig. 4).

The steady state of a diode pump occurs[5]) when the charge fed into the tank capacitor C_t per unit time is equal to the current that flows through the load resistor R_p. For the circuit of fig. 4 this condition can be stated as

$$\tfrac{1}{2} n\, C_f (V_H - V_L - V_{D1} - V_{D2} - V_p) = V_p/R_p, \tag{8}$$

where n is the counting rate ($\frac{1}{2}n$ is the number of square waves at the output of the flip-flop IC4), C_f is the value of the feed capacitor of the pump, V_H is the logic "high" voltage level of IC4 [$V_H = 3.75$ V at $T = 25\,°C$, $V_{cc} = 5$ V and zero fanout[3])], V_L is the logic "low" voltage level of IC4 [$V_L = 0.2$ V for $0\,°C \leq T \leq 70\,°C$ and $4.75\ \text{V} \leq V_{cc} \leq 5.25\ \text{V}$[3])], and V_{D1} and V_{D2} are the forward bias voltages of D1 and D2 at the end of their respective conduction cycles, i.e. one half of the mentioned square wave each. The values of V_{D1} and V_{D2} depend on the diode types applied, on the current and of course on the temperature.

At the end of the conduction cycle of each diode, and provided that $1/n$ is much longer than the charging- (through D1) or the discharging (through D2) time constants of C_f, yet n is sufficiently high so as to ensure saturation of the pump, currents of the order of a few μA will flow through D1 and D2. Under these conditions, the forward bias voltage of the diode types 1N137A applied for the pumps is 0.5 V at 25 °C.

The steady state pump voltage obtained from eq. (8) is

$$V_p = \frac{\frac{1}{2} n\, C_f (V_H - V_L - V_{D1} - V_{D2})}{\frac{1}{2} n\, C_f + 1/R_p}. \tag{9}$$

Assuming that the pump is saturated,

$$\tfrac{1}{2} n \gg \frac{1}{C_f R_p},$$

therefore

$$\tfrac{1}{2} n\, C_f \gg \frac{1}{R_p}. \tag{10}$$

Introducing condition (10) into eq. (9), the output voltage of a saturated pump is

$$V_{p_{sat}} = V_H - V_L - V_{D1} - V_{D2}. \tag{11}$$

Calculation of $V_{p_{sat}}$ making use of the numerical values and at the conditions discussed above yields

$$V_{p_{sat}} = 2.55\ \text{V}, \quad (\text{at } T = 25\,°C). \tag{12}$$

Taking the derivative of $V_{p_{sat}}$ of eq. (11) with respect to temperature,

$$\frac{dV_{p_{sat}}}{dT} = \frac{dV_H}{dT} - \frac{dV_L}{dT} - \frac{dV_{D1}}{dT} - \frac{dV_{D2}}{dT}, \tag{13}$$

where each of the right hand terms can be evaluated as follows.

The logic "high" voltage level of the TTL series 74 applied for IC4 depends on supply voltage and on

temperature according to the following (approximate) expression[3])

$$V_H = 3.75\ \text{V} + (V_{cc} - 5\ \text{V}) + 4.0 \times 10^{-3}(T - 25°\text{C})\ \text{V/°C}, \quad (14)$$

with $0°\text{C} \leq T \leq 70°\text{C}$, $4.75\ \text{V} \leq V_{cc} \leq 5.25\ \text{V}$, and zero fanout.

From eq. (14), the first right hand term of eq. (13) is

$$\frac{dV_H}{dT} = 4.0\ \text{mV/°C}. \quad (15)$$

The second right hand term of eq. (13) can be assumed to be zero within the TTL series 74 rated limits of supply voltage and temperature[3]). Hence,

$$\frac{dV_L}{dT} = 0. \quad (16)$$

The third and fourth right hand terms are somehow difficult to calculate. A rather accurate expression of the forward bias voltage of semiconductor diodes at constant current as a function of temperature was given by Brugler[6]), but neither D1 nor D2 work under constant current conditions. However, if the different pumps of the array are designed so that the charging or discharging times are much shorter than the period at which each pump is saturated (which is usually the case), the average current through each diode is of the same order of magnitude as that at the end of its conduction time. The assumption that D1 and D2 work under constant currents of few μA can therefore lead to a good approximation. Taking the derivative of $V_D(T)$ as given in ref. 6 with respect to temperature and neglecting low influence terms yields

$$\frac{dV_D}{dT} = -\frac{V_G - V_{D_0}}{T_0}, \quad (17)$$

where V_G is the forbidden band gap voltage of the semiconductor material extrapolated to 0K ($V_G = 1.205$ V for silicon) and V_{D_0} is the forward bias voltage of the diode at a constant current I_D and at temperature T_0. Formally similar expressions of dV_D/dT can be found in refs. 7 and 8. Since V_{D_0} is proportional to T_0 and $\ln J_D$, where $J_D = I_D/A$ is the current density at the junction of area A, the rate of change of V_D with temperature decreases with increasing current and temperature. Introducing the value of $V_{D1} = V_{D2} = 0.5$ V at 25°C already used for eq. (12) into eq. (17) gives

$$\frac{dV_{D1}}{dT} = \frac{dV_{D2}}{dT} = -2.36\ \text{mV/°C}. \quad (18)$$

Introducing the values given in eqs. (15), (16) and (18) into eq. (13),

$$\frac{dV_{psat}}{dT} = +8.72\ \text{mV/°C}. \quad (19)$$

The temperature dependence of the output voltage of a non-saturated pump can be evaluated as follows. Introducing eq. (11) into eq. (9),

$$V_p = \frac{\frac{1}{2} n\, C_f\, V_{psat}}{\frac{1}{2} n\, C_f + (1/R_p)}. \quad (20)$$

Taking the derivative of V_p with respect to temperature and assuming that neither C_f nor R_p are temperature dependent,

$$\frac{dV_p}{dT} = \frac{\frac{1}{2} n\, C_f}{\frac{1}{2} n\, C_f + (1/R_p)} \cdot \frac{dV_{psat}}{dT}. \quad (21)$$

It follows from eqs. (20) and (21) that

$$\frac{1}{V_p} \cdot \frac{dV_p}{dT} = \frac{1}{V_{psat}} \cdot \frac{dV_{psat}}{dT}. \quad (22)$$

That is to say, the relative rate of change of the pump voltage with respect to temperature does not depend on the counting rate and its value is approximately

$$\frac{1}{V_p} \cdot \frac{dV_p}{dT} = +0.342\ \text{%/°C}, \quad (23)$$

where use has been made of the numerical values given in eqs. (12) and (19) and of eq. (22).

The relative rate of change of the output voltage V_0 with temperature can be evaluated now. The output voltage is

$$V_0 = \sum_{i=1}^{p} V_{p_i} \frac{R_f}{R_{p_i}}, \quad (24)$$

where p is the total number of pumps of the array. Taking the derivative of V_0 of eq. (24) with respect to temperature, and neglecting the temperature dependence of the ratios R_f/R_{p_i},

$$\frac{dV_0}{dT} = \sum_{i=1}^{p} \frac{dV_{p_i}}{dT} \cdot \frac{R_f}{R_{p_i}}. \quad (25)$$

Dividing this equation by eq. (24) and introducing the value of dV_p/dT of eq. (23) into the result, it is found that

$$\frac{1}{V_0}\frac{dV_0}{dT} = \frac{1}{V_p}\frac{dV_p}{dT} = \frac{1}{V_{psat}}\frac{dV_{psat}}{dT} = 0.342\ \text{%/°C}. \quad (26)$$

That is, the relative rate of change of the sum of pump voltages with respect to temperature is equal to that of a single pump, be it saturated or not, it does not depend on the counting rate or on the pumps' time constants and in first approximation it does not depend on temperature. Note also that the load resistors R_{p_i} need not be all equal; their nonequality is particularly useful for the linearization of the V_0 versus log n transfer characteristic of a pump array[5]).

Appendix 2

Calculation of the rate of change of V_{cc} with temperature necessary to cancel temperature induced variations of the counting rate meter.

It is required that

$$\frac{dV_0}{dT} = 0. \tag{27}$$

It follows from eq. (26) that

$$\frac{dV_p}{dT} = \frac{dV_{psat}}{dT} = 0. \tag{28}$$

Imposing this condition on eq. (13),

$$\frac{dV_H}{dT} - \frac{dV_L}{dT} - \frac{dV_{D1}}{dT} - \frac{dV_{D2}}{dT} = 0. \tag{29}$$

With the arrangement of fig. 3 to provide the temperature dependent supply voltage V_{cc}, the logic "high" voltage level V_H depends on temperature directly and also indirectly through the change of V_{cc} with temperature. The first term of eq. (29) can be written as

$$\frac{dV_H}{dT} = \frac{\partial V_H}{\partial T} + \frac{\partial V_H}{\partial V_{cc}} \frac{dV_{cc}}{dT}. \tag{30}$$

From eq. (14), the values of the partial derivatives are

$$\frac{\partial V_H}{\partial T} = 4.0\ \text{mV/°C} \quad \text{and} \quad \frac{\partial V_H}{\partial V_{cc}} = 1. \tag{31}$$

Introducing dV_H/dT of eq. (30) into eq. (29) and solving for dV_{cc}/dT,

$$\frac{dV_{cc}}{dT} = -8.72\ \text{mV/°C}. \tag{32}$$

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